## REMARKS

Claims 1, 3 and 4 are pending. Claim 1, the only independent claim, has been amended. Claim 2 has been cancelled without prejudice.

Claims 1-4 were rejected under 35 U.S.C. § 102(b) as anticipated by Tamura (EP 0 640 916 A2). Applicant submits that claim 1 is patentable over Tamura for at least the following reasons.

Claim 1 is directed to a computer system comprising a CPU for operating with pipe-line processing, a ROM (e.g., 52) storing a program to be executed by the CPU (e.g., 51), and a plurality of ROM correction units (e.g., 53) each including a first storage unit (e.g., 31) for storing a subject address of an original instruction group in the program having a bug therein, a second storage unit (e.g., 60) for storing a modified instruction group for replacing the original instruction group by the modified instruction group having a branch address, a comparator (e.g., 34) for comparing a current address of a current instruction read from the ROM (e.g., 52) against the subject address, a selector (e.g., 36) for selecting the current address or the branch address based on a result of the comparison by the comparator (e.g., 34), a flag generator (e.g., 33) for setting a ROM correction flag when the selector (e.g., 36) selects the branch address. One of the ROM correction units delivers the ROM correction flag through a data bus (e.g., bus 56 in Figure 2).

In the claim invention, ROM stores a program for an execution stage, the execution stage being a stage in which the branch command is executed.

Tamura, on the other hand, shows an instruction fetch stage, which fetches an instructions before the branch command is executed. Tamura shows in Figure 6 that an enable flag 15 indicates whether or not the ROM correction unit is enabled, which may be seen to correspond to the control signal 102 in Figure 4 of the present invention.

In the present invention, the ROM correction flag 108 indicates that the current address jumps to the branch address as a result of the function of the enabled ROM correction unit. The CPU receives the branch instruction (JMP) to execute the jump instruction; a flag is set after the execution of the jump instruction. The flag is therefore assigned to identify the execution of the jump instruction by the CPU, and the flag is not assigned to execution of the other current instruction.

For at least the reasons delineated above, claim 1 is believed patentable over Tamura. Moreover, the Examiner took the position regarding Tamura that "since the instruction executing unit outputs data (signals) across a bus . . . , the flag is also outputted across the bus." This surmise was apparently based upon the fact that the instruction executing unit controls the outputting of the enable flag 15. However, while the instruction executing unit *controls* the outputting of the enable flag 15, the enable flag itself is *not* indicated as being delivered through a data bus.

In fact, as can be seen in Figure 6 of Tamura, the enable flag is connected to the latch by a signal line. There is no indication that the flag is outputted across *any* data bus, and certainly not across the data bus between the instruction executing unit and the selector, contrary to the position taken at page 3 of the Office Action. The fact that outputting of the enable flag is *under the control of* the instruction executing unit is not a teaching that the flag itself is delivered through a data bus, especially when that is contradicted by Figure 6. For at least the foregoing reasons, it is believed clear that Tamura does not teach the features of claim 1.

For at least the reasons discussed above, claim 1 is believed patentable over Tamura. Withdrawal of the rejection is requested.

The other claims in this application are each dependent from the independent claim discussed above and are therefore believed patentable for the same reasons. Since each dependent claim is also deemed to define an additional aspect of the invention, however, the

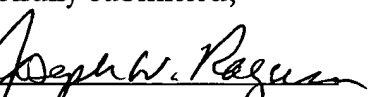
individual reconsideration of the patentability of each on its own merits is respectfully requested.

This Amendment After Final Rejection is believed clearly to place this application in condition for allowance and its entry is therefore believed proper under 37 C.F.R. § 1.116. In any event, however, entry of this Amendment After Final Rejection, as an earnest effort to advance prosecution and reduce the number of issues, is respectfully requested.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

Dated: June 3, 2004

Respectfully submitted,

By 

Joseph W. Ragusa
Registration No.: 38,586
DICKSTEIN SHAPIRO MORIN &
OSHINSKY LLP
1177 Avenue of the Americas
41st Floor
New York, New York 10036-2714
(212) 835-1400
Attorney for Applicant